1. (Original) A method of fabricating a semiconductor device with negative differential conductance or transconductance, comprising:

a first step of etching a single crystal silicon layer of an SOI substrate consisting sequentially of a silicon support, a buried oxide film and the single crystal silicon layer so as to form source and drain regions which are spaced apart from each other and a channel region which is connected with the source and drain regions and has a fine line width;

a second step of implanting impurity ions into the source, channel, and drain regions with their density being higher than the effective density of states at which electrons or holes can exist so that the channel is doped with the impurity ions;

a third step of forming a first insulation film on the source, channel and drain regions and the buried oxide film, and etching the first insulation film so as to form sidewall spacers on side surfaces of the source, channel and drain regions and then forming a second insulation film on the exposed silicon surface including the source, channel and drain regions so as to form a gate insulation film on the channel region;

a fourth step of depositing a gate material on the entire surface including the second insulation film and forming a gate having a fine line width in a direction normal to the channel region by etching the deposited gate material; and

a fifth step of implanting impurity ions, having opposite polarity to that of the impurity ions implanted in the second step, into the source and drain regions.

2. (Original) The method as claimed in claim 1, wherein the impurity ions implanted in the second step are P-type impurity ions, and the impurity ions implanted in the fifth step are N-type impurity ions.

3. (Original) The method as claimed in claim 1, wherein the impurity ions implanted in the second step are N-type impurity ions, and the impurity ions implanted in the fifth step are P-type impurity ions.

4. (Amended herein) The method as claimed in claim 2 ~~or 3~~, wherein the P-type impurity ions are ones selected from the group consisting of B, BF_2^+ and In, and the N-type impurity ions are ones ~~ONONOO~~ selected from the group consisting of As_2^+, As and P.

5. (Original) The method as claimed in claim 1, wherein the silicon single crystal at the first step and the gate material at the fourth step are etched with an E-beam lithography method or a fine patterning technique using sidewalls.

6. (Original) The method as claimed in claim 1, wherein the gate material at the fourth step is polycrystalline or amorphous silicon.

7. (Original) The method as claimed in claim 1, further comprising the step of, between the fourth and fifth steps, forming an insulation film for covering the entire surface including the source, gate and drain regions and the buried oxide film and etching the insulation film so as to form sidewall spacers in side surfaces of the gate.

8. (Original) The method as claimed in claim 1, wherein the material of the insulation film are ones selected from the group consisting of SiO_2 and SiN.

9. (Amended herein) A method for fabricating a semiconductor device with negative differential conductance or transconductance, comprising:

a first step of etching the single crystal silicon layer of an SOI substrate consisting sequentially of a silicon support, a buried oxide film and the single crystal silicon layer so as to form source and drain regions which are spaced apart from each other and a channel region which is connected with the source and drain regions and has a fine line width;

a second step of implanting impurity ions into the source, channel and drain regions with their density being higher than the effective density of states at which electrons or holes can exist so that the source and drain regions are doped with the impurity ions;

a third step of forming a first insulation film on the source, channel and drain regions and the buried oxide film, and etching the first insulation film so as to form sidewall spacers of the source, channel and drain regions;

a fourth step of depositing a second insulation film on the entire surface including the source, channel and drain regions ~~Regions~~, the sidewall spacers and the buried oxide film, and exposing the channel region by etching the second insulation film in a direction normal to the channel region;

a fifth step of implanting impurity ions, having opposite polarity to that of the impurity ions implanted in the second step, into the channel region with their density being higher than the effective density of states; and

a sixth step of depositing a gate insulation film on the channel region, and then forming a gate by depositing a gate material on the channel region and the gate insulation film.

10. (Original) The method as claimed in claim 9, wherein the sixth step further comprises the step of planarizing the deposited gate material.

11. (Original) The method as claimed in claim 10, wherein the planarizing process is an etchback process or a chemical mechanical polishing (CMP) process.

12. (Original) The method as claimed in claim 9, wherein the material of the first and second insulation film are ones selected from the group consisting of SiO_2 and SiN.

13. (Original) The method as claimed in claim 9, wherein the silicon single crystal at the first step and the gate material at the sixth step are etched with an E-beam lithography method or a fine patterning technique using sidewalls.

14. (Original) the method as claimed in claim 9, wherein the gate material deposited in the sixth step is polycrystalline or amorphous silicon.

15. (New) The method as claimed in claim 3, wherein the P-type impurity ions are ones selected from the group consisting of B, BF_2^+ and In, and the N-type impurity ions are ones selected from the group consisting of As_2^+, As and P.